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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,329	02/24/2004	Chun-Wen Cheng	NAUP0547USA	2328

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NORTH AMERICA INTERNATIONAL PATENT OFFICE (NAIPC)
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EXAMINER	
DOAN, THERESA T	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H'D

Office Action Summary	Application No.	Applicant(s)	
	10/708,329	CHENG, CHUN-WEN	
	Examiner	Art Unit	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Om et al. (U.S Pat. 5,200,354) in view of Chen (U.S 20040129965).

Regarding claims 1-2, Om (figure 1) discloses a deep trench capacitor memory cell 41, comprising:

a second conductivity type semiconductor substrate 40 with a main surface (column 6, lines 43-45);

a second conductivity type ion implantation well 15 (column 13, lines 65-68 and column 14, lines 1-4) with a well junction depth located on the main surface;

a gate dielectric layer 10 located on the ion implantation well 15 (column 7, line 20);

a gate 8 located on the gate dielectric layer 10 (see figure 1);

a heavily doped S/D region 11 of the first conductivity type disposed at one side of the gate 8 in the ion implantation well 15 (see figure 1);

a lightly doped drain (LDD) region 19 of the first conductivity type disposed at the other side of the gate 8 in the ion implantation well 15 (see figure 1); and

a deep trench capacitor 41 vertically extending into the main surface through the well 15 junction depth of the ion implantation well to a pre-selected depth, wherein the deep trench capacitor 41, which is fabricated adjacent to the LDD region 19, comprises an ion out diffusion well 14 of the second conductivity type that is formed at a lower portion of the deep trench capacitor and is merged with the ion implantation well 15, and a conductive electrode pillar (column 7, lines 7-8) electrically isolated from the LDD region 19, the ion implantation well 15, and the ion out diffusion well 14 by a capacitor dielectric layer 12 and a trench top insulation layer 9 (see figure 1).

Om discloses the semiconductor substrate 40 is a second conductivity type, but does not disclose the semiconductor substrate 40 is a first conductivity type.

However, Chen (figure 10) discloses a substrate 100 includes P-substrate or N-substrate that may be used with appropriately charging conductivities (see paragraph [0028]). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the substrate with either P or N conductivity because as taught by Chen, such P or N conductivity type of substrate would provide the same result of supporting the electronic components.

Regarding claim 3, Om discloses wherein the ion out diffusion well 14 has a top end located a depth W_d of over 4000 angstroms below the main surface of the substrate (see figures 1-2, column 9, line 55).

Regarding claim 4, Om discloses the deep trench capacitor 41 vertically extends into the main surface through the well junction depth of the ion implantation well to a depth that is deeper than 3 micrometers (figure 2, column 8, line 8).

Regarding claim 5, Om discloses the capacitor dielectric layer 12 is an oxide-nitride-oxide (ONO) dielectric layer (figure 5H, column 7, lines 1-5).

Regarding claim 6, Om discloses wherein the trench top insulation layer 9 is made of silicon oxide (figure 1, column 7, lines 10-15).

Regarding claim 7, Om (figure 1) discloses wherein the trench top insulation layer 9 is disposed atop the conductive electrode pillar 13 but does not disclose an insulation layer thickness of about 100-400 angstroms. It would have been obvious to form an insulation layer thickness of about 100-400 angstroms in Om's structure, since it has been held when the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Applicant can rebut a prima facie case of obviousness based on

ranges by showing unexpected results or the criticality of the claimed range. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claim. In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP 716.02 - 716.02(g) for a discussion of criticality and unexpected results. There is nothing in the present application to indicate that the claimed of the insulation layer thickness of about 100-400 angstroms is critical.

3. Claims 8-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Om et al. (U.S Pat. 5,200,354) in view of Chen (U.S 20040129965) and further in view of El-Kareh et al. (U.S Pat. 5,805,494).

Regarding claim 8, the discussions with respect to the combination of Om and Chen in conjunction with rejection of claim 1 is herein incorporated by reference. Neither Om nor Chen discloses the deep trench capacitor, which is 1T-SRAM.

However, El-Kareh discloses the trench capacitor structure can be used in DRAM or SRAM (figure 10 and column 5, lines 8-9). Accordingly, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply a deep-trench capacitor of Om into SRAM, as taught by El-Kareh, because such a deep-trench 1T-SRAM structure would provide the soft-error immunity in for static random access memory cell (column 1, lines 9-13). The

recitation of using "a deep-trench 1T-SRAM device" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Regarding claim 9, Om discloses wherein a trench top insulation layer 9 is disposed atop the conductive electrode pillar 13 (see figure 1).

Regarding claim 10, Om discloses wherein a share contact plug penetrates through the trench top insulation layer and is electrically connected to the conductive electrode pillar (see figure 3).

Regarding claim 11, Om discloses wherein the trench top insulation layer 9 is made of silicon oxide (figure 1, column 7, lines 10-15).

Regarding claim 12, Om (figure 1) discloses wherein the trench top insulation layer 9 is disposed atop the conductive electrode pillar 13 but does not disclose an insulation layer thickness of about 100-400 angstroms. It would have been obvious to form an insulation layer thickness of about 100-400 angstroms in

Om's structure, since it has been held when the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Applicant can rebut a prima facie case of obviousness based on ranges by showing unexpected results or the criticality of the claimed range. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claim. In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP 716.02 - 716.02(g) for a discussion of criticality and unexpected results. There is nothing in the present application to indicate that the claimed of the insulation layer thickness of about 100-400 angstroms is critical.

Regarding claim 13, Om discloses the capacitor dielectric layer 12 is an oxide-nitride-oxide (ONO) dielectric layer (figure 5H, column 7, lines 1-5).

Regarding claim 14, Om discloses the deep trench capacitor 41 vertically extends into the main surface through the well junction depth of the ion implantation well to a depth that is deeper than 3 micrometers (figure 2, column 8, line 8).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TD
April 28, 2005.

PHAT X. CAO
PRIMARY EXAMINER